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10/824,504	04/15/2004	Yuichiro Morita	500.40687CX1	6566

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ANTONELLI, TERRY, STOUT & KRAUS, LLP
1300 NORTH SEVENTEENTH STREET
SUITE 1800
ARLINGTON, VA 22209-3873

EXAMINER	
SAVLA, ARPAN P	
ART UNIT	**PAPER NUMBER**
2185	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/824,504	MORITA ET AL.	
	Examiner	Art Unit	
	Arpan P. Savla	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on April 5, 2007 has been entered.

Response to Amendment

This Office action is in response to Applicant's communication filed April 5, 2007 in response to the Office action dated November 6, 2006. Claims 1-5 have been amended. Claims 1-5 are pending in this application.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nguyen (U.S. Patent 5,732,236).

3. **As per claim 1**, Nguyen discloses memory controller comprising:

means for receiving, from a processor (col. 2, lines 62-66; col. 3, lines 25-27; Fig. 1, element 10), a request for access to a dynamic random access memory (col. 4, lines 21-26; Fig. 2a, element 38) having a data storage area divided into a plurality of banks each divided into a plurality of pages (col. 3, lines 8-10 and 35-37; Fig. 1, elements 11, 30, 32, 34, and 36); *It should be noted that pg. 15, lines 3-5 of Applicant's specification appear to define this means as an "access arbiter." Nguyen's "prioritizer" is equivalent to Applicant's "access arbiter." It should also be noted that even though the "requesting circuits" comprise multiple devices, when all of the multiple devices are taken as a whole they comprise the "microprocessor" (col. 2, lines 62-66), which is in turn a solitary requesting device. Therefore, Nguyen's "microprocessor" is equivalent to Applicant's "processor."*

Nguyen does not expressly disclose that the dynamic random access memory is a single memory;

wherein said plurality of banks are formed on a single chip, and wherein said random access memory is adapted to share control signals received by said random access memory, from said memory control means, among said plurality of banks.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to form the dynamic random access memory as a single memory and form the plurality of banks on a single chip. It should also be noted that within this modified construction of Nguyen the control signals 26 received by system memory 11 (i.e. the single dynamic random access memory) would be shared throughout the

system memory 11 as a whole in the same manner as control signals RAS#, CAS#, WE#, CS# are shared throughout DRAM 7 in the instant application.

It has been held to be within the general skill of a worker in the art to make plural parts unitary as a matter of obvious engineering choice. See *In re Larson*, 144 USPQ 347 (CCPA 1965), *In re Lockart*, 90 USPQ 214 (CCPA 1951), and *Howard v. Detroit Stove Works*, 150 U.S. 164 (1893).

Therefore, it would have been obvious to modify Nguyen for the benefit of obtaining the invention as specified in claim 1.

4. **As per claim 2**, Nguyen discloses memory controller comprising:

means for receiving, from a processor (col. 2, lines 62-66; col. 3, lines 25-27; Fig. 1, element 10), a request for access to a dynamic random access memory (col. 4, lines 21-26; Fig. 2a, element 38) having a data storage area divided into a plurality of banks each divided into a plurality of pages (col. 3, lines 8-10 and 35-37; Fig. 1, elements 11, 30, 32, 34, and 36); *Please see the italicized citation notes for the first limitation of claim 1 above.*

and memory control means for activating a page to be accessed (col. 5, lines 49-52; col. 3, lines 39-48; Fig. 2b, element 84), based on said access request from said processor (col. 3, lines 27-32 and 55-59), and executing, before a next request for access to a page to be accessed subsequently by said processor, precharge of a bank corresponding to said page to be accessed subsequently (col. 4, lines 5-13; col. 8, lines 3-11; Fig. 3b). *Please see the italicized citation notes for the second limitation of claim 1 above.*

Nguyen does not expressly disclose that the dynamic random access memory is a single memory;

wherein said plurality of banks are formed on a single chip, and wherein said random access memory is adapted to share control signals received by said random access memory, from said memory control means, among said plurality of banks.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to form the dynamic random access memory as a single memory and form the plurality of banks on a single chip. It should also be noted that within this modified construction of Nguyen the control signals 26 received by system memory 11 (i.e. the single dynamic random access memory) would be shared throughout the system memory 11 as a whole in the same manner as control signals RAS#, CAS#, WE#, CS# are shared throughout DRAM 7 in the instant application.

It has been held to be within the general skill of a worker in the art to make plural parts unitary as a matter of obvious engineering choice. See *In re Larson*, 144 USPQ 347 (CCPA 1965), *In re Lockart*, 90 USPQ 214 (CCPA 1951), and *Howard v. Detroit Stove Works*, 150 U.S. 164 (1893).

Therefore, it would have been obvious to modify Nguyen for the benefit of obtaining the invention as specified in claim 2.

5. **As per claim 3**, Nguyen discloses a memory controller for use with a processor and a dynamic random access memory, comprising:

a terminal (col. 4, lines 21-26; Fig. 2a, element 38) adapted to receive a request for access from said processor to a dynamic random access memory having a data

storage area divided into a plurality of banks each divided into a plurality of pages (col. 3, lines 8-10 and 35-37; Fig. 1, elements 11, 30, 32, 34, and 36); *It should be noted that Nguyen's "prioritizer" is equivalent to Applicant's "terminal." Also, please see the italicized citation notes for the first limitation of claim 1 above.*

and memory control means for issuing an active command for activating a page to be accessed (col. 5, lines 49-52; col. 3, lines 39-48; Fig. 2b, element 84), based on said access request from said processor (col. 3, lines 27-32 and 55-59), and issuing a precharge command for executing, before a next request for access to a page to be accessed subsequently, precharge of said page to be accessed subsequently (col. 4, lines 5-13; col. 8, lines 3-11; Fig. 3b). *It should be noted that in any computer system it is inherently required that a controller/processor issue a "command" in order for any action (such as activating a page or executing a precharge) to be carried out. Also, please see the italicized citation notes for the second limitation of claim 1 above.*

Nguyen does not expressly disclose that the dynamic random access memory is a single memory;

wherein said plurality of banks are formed on a single chip, and wherein said random access memory is adapted to share control signals received by said random access memory, from said memory control means, among said plurality of banks.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to form the dynamic random access memory as a single memory and form the plurality of banks on a single chip. It should also be noted that within this modified construction of Nguyen the control signals 26 received by system memory 11

(i.e. the single dynamic random access memory) would be shared throughout the system memory 11 as a whole in the same manner as control signals RAS#, CAS#, WE#, CS# are shared throughout DRAM 7 in the instant application.

It has been held to be within the general skill of a worker in the art to make plural parts unitary as a matter of obvious engineering choice. See *In re Larson*, 144 USPQ 347 (CCPA 1965), *In re Lockart*, 90 USPQ 214 (CCPA 1951), and *Howard v. Detroit Stove Works*, 150 U.S. 164 (1893).

Therefore, it would have been obvious to modify Nguyen for the benefit of obtaining the invention as specified in claim 3.

6. **As per claim 4**, Nguyen discloses a memory controller for use with a processor and a dynamic random access memory, comprising:

a terminal (col. 4, lines 21-26; Fig. 2a, element 38) for receiving a request for access from said processor to a dynamic random access memory having a data storage area divided into a plurality of banks each divided into a plurality of pages (col. 3, lines 8-10 and 35-37; Fig. 1, elements 11, 30, 32, 34, and 36); *Please see the italicized citation notes for the first limitations of both claim 1 and claim 3 above.*

and memory control means for issuing an active command for activating a page to be accessed (col. 5, lines 49-52; col. 3, lines 39-48; Fig. 2b, element 84), based on said access request from said processor (col. 3, lines 27-32 and 55-59), and issuing a precharge command for executing, before a next request for access to a page to be accessed subsequently, precharge of a bank corresponding to said page to be

accessed subsequently (col. 4, lines 5-13; col. 8, lines 3-11; Fig. 3b). *Please see the italicized citation notes for the second limitations of both claim 1 and claim 3 above.*

Nguyen does not expressly disclose that the dynamic random access memory is a single memory;

wherein said plurality of banks are formed on a single chip, and wherein said random access memory is adapted to share control signals received by said random access memory, from said memory control means, among said plurality of banks.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to form the dynamic random access memory as a single memory and form the plurality of banks on a single chip. It should also be noted that within this modified construction of Nguyen the control signals 26 received by system memory 11 (i.e. the single dynamic random access memory) would be shared throughout the system memory 11 as a whole in the same manner as control signals RAS#, CAS#, WE#, CS# are shared throughout DRAM 7 in the instant application.

It has been held to be within the general skill of a worker in the art to make plural parts unitary as a matter of obvious engineering choice. See *In re Larson*, 144 USPQ 347 (CCPA 1965), *In re Lockart*, 90 USPQ 214 (CCPA 1951), and *Howard v. Detroit Stove Works*, 150 U.S. 164 (1893).

Therefore, it would have been obvious to modify Nguyen for the benefit of obtaining the invention as specified in claim 4.

7. **As per claim 5**, Nguyen discloses a memory controller comprising:

a terminal (col. 4, lines 21-26; Fig. 2a, element 38) adapted to receive, from a processor, a request for to a dynamic random access memory having a data storage area divided into a plurality of banks each divided into a plurality of pages (col. 3, lines 8-10 and 35-37; Fig. 1, elements 11, 30, 32, 34, and 36); *Please see the italicized citation notes for the first limitations of both claim 1 and claim 3 above.*

and a memory control unit adapted to activate a page to be accessed (col. 5, lines 49-52; col. 3, lines 39-48; Fig. 2b, element 84), based on said access request from said processor (col. 3, lines 27-32 and 55-59), and to execute, before a next request for access to a page to be accessed subsequently by said processor, precharge of said page to be accessed subsequently (col. 4, lines 5-13; col. 8, lines 3-11; Fig. 3b). *It should be noted that Nguyen's "plurality of memory bank controllers" is equivalent to Applicant's "memory control unit." Also, please see the italicized citation notes for the second limitation of claim 1 above.*

Nguyen does not expressly disclose that the dynamic random access memory is a single memory;

wherein said plurality of banks are formed on a single chip, and wherein said random access memory is adapted to share control signals received by said random access memory, from said memory control means, among said plurality of banks.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to form the dynamic random access memory as a single memory and form the plurality of banks on a single chip. It should also be noted that within this modified construction of Nguyen the control signals 26 received by system memory 11

(i.e. the single dynamic random access memory) would be shared throughout the system memory 11 as a whole in the same manner as control signals RAS#, CAS#, WE#, CS# are shared throughout DRAM 7 in the instant application.

It has been held to be within the general skill of a worker in the art to make plural parts unitary as a matter of obvious engineering choice. See *In re Larson*, 144 USPQ 347 (CCPA 1965), *In re Lockart*, 90 USPQ 214 (CCPA 1951), and *Howard v. Detroit Stove Works*, 150 U.S. 164 (1893).

Therefore, it would have been obvious to modify Nguyen for the benefit of obtaining the invention as specified in claim 5.

Response to Arguments

8. Applicant's arguments with respect to **claims 1-5** have been considered but are moot in view of the new ground of rejection above.

Conclusion

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by MPEP 707.70(i):

CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, **claims 1-5** have received a first action on the merits and are subject of a first action non-final.

RELEVANT ART CITED BY THE EXAMINER

The following prior art made of record and not relied upon is cited to establish the level of skill in Applicant's art and those arts considered reasonably pertinent to Applicant's disclosure. See MPEP 707.05(e).

1. U.S. Patent 5,301,278 (Bowater et al.) discloses sharing control signals received by a random access memory, from a memory control means, among a plurality of banks.

2. U.S. Patent 6,009,489 (Mergard) discloses sharing control signals received by a random access memory, from a memory control means, among a plurality of banks.

3. U.S. Patent 6,327,192 (Lee) discloses a single dynamic random access memory with multiple banks.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arpan P. Savla whose telephone number is (571) 272-1077. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Arpan Savla
Art Unit 2185
May 23, 2007

SANJIV SHAH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100